REMARKS

Claims 1-10, 13-18, 20-22 and 24 remain pending in the instant application. Claims 1-10, 13-18, 20-22 and 24 presently stand rejected. Claims 14, 15, 21, 24, and 25 are amended herein. No new matter has been added. Entry of this amendment and reconsideration of the pending claims are respectfully requested.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 7-9, 14-17, 20-22, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Banerjee (US 6,820,127 B2) in view of Brustoloni et al. (US 6,625,149 B1) and Ganfield (US 2004/0218631).

Claims 2-6, 10, 13, 18, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Banerjee in view of Brustoloni et al. and Ganfield as applied to claims 1, 8, 14, and 25 above, and further in view of Kaniyar et al (US 7,219,121).

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.

Claim 1 as previously presented recites:

> A method comprising: receiving a packet at a network device; pre-fetching a protocol control block (PCB) associated with the packet into a cache of a selected processing unit; queuing the packet for processing; **pre-fetching a header associated with the packet into the cache of the selected processing unit**; and

retrieving the PCB from the cache of the selected processing unit when the selected processing unit is ready to process the packet.

In contrast, the combined references do not teach or suggest (at least) the above-emphasized portion of the claim. The Office Action alleges (in page 12, in the Response to Arguments) that Banerjee in no uncertain terms teaches that cache memory can be shared between processors or can be unique to a processor as illustrated in Banerjee's (5:27-32). However, in the cited portion, Banerjee discloses that the PCB cache of each processor is small and (thus) contains the most frequently accessed PCBs (5:29-32). Banerjee does not teach or fairly suggest sharing of a cache stored with each processor with other processors.

Instead, Banerjee teaches away from sharing of a cache stored with each processor with other processors because of the small size of the cache stored with each processor: because the cache is small, (only) a limited number of PCBs (the most frequently used) can be stored. This teaches away from sharing limited resources from other processors. Sharing a local cache with other processors would increase the number of cache misses, increase cache latency and contention (with other processors accessing the cache across busses that are typically slower than the local processor bus). Thus sharing the local cache with other processors would render the cache stored for a selected processor to be unsuitable for its intended task of speeding performance of the local cache for the selected processor. Thus, the caches of selected processors are not shared by other processors.

The Office Action further reasons that Brustoloni teaches that a header associated with an incoming or received packet can be placed in a cache memory for speedy

retrieval and the fact that the cache is shared or not is irrelevant as it is already taught by Banerjee. As discussed above, Banerjee does not teach or fairly suggest sharing the cache of a selected processor. Furthermore, Brustoloni in the cited portion (Fig. 3, item 80) teaches queuing the received packet for processing. Thus Brustoloni teaches queuing (in general) the entire packet and every received packet. Modifying the cache of Banerjee to queue each and every packet from other processors (as taught by Brustoloni) would render the cache of Banerjee unsuitable for its intended purpose, a fortiori, for at least the reasons discussed above for sharing queues of PCBs between different processors. For example, the cache of Banerjee is insufficient to hold PCBs for all packets, much less holding the packets themselves. Storing the entire packet of every received packet would thus defeat the purpose of providing quick access of information needed (such as the PCB) to process a packet. Thus Brustoloni fails to overcome the deficiency of Banerjee. For the above reasons, at least, applicants traverse the alleged motivation to combine Brustoloni with Banerjee

The Office Action further alleges that Ganfield discloses pre-fetching a header associated with the packet in the cache of the selected processing unit. Instead, Ganfield (paragraphs 38 and 39) storing a length (L) from a PCB in a buffer descriptor cache in header information 526. Thus the information being stored is not the packet header (see dependent claim 3 of the instant application), and is instead derived from the PCB. Thus Ganfield fails to overcome the deficiencies of Brustoloni and Banerjee, either singly or in motivated combination. Accordingly claim 1 is believed to be allowable.

Claim 14, as amended, recites:

14. (Currently Amended) An article of manufacture comprising: a machine accessible medium including content that when accessed by a machine causes the machine to: receive a packet; pre-fetch a protocol control block (PCB) associated with the packet and a packet header of the packet into a cache of a processing unit; queue the packet for processing; retrieve the PCB from the cache when the processing unit is ready to process the packet; and to pre-fetch a PCB for a packet to be sent when the to-be-sent packet is queued for transmission across a network wherein the PCB for the to-be-sent packet is pre-fetched in response to a send request being initiated for the to-be-sent packet.

In addition to the reasons stated above with respect to claim 1, claim 14 is also believed to be allowable because the cited art fails to teach or suggest the above emphasized limitations. For example, Banerjee fails to pre-fetch a PCB for a to-be-sent packet for transmission across a network. Instead, for example, Banerjee teaches (Fig. 7, step 718) delivery to an appropriate user process. Thus claim 14 is believed to be allowable.

Claim 21 is believed to be allowable for at least reasons stated above. Dependent claims are at least allowable for the reasons from which they depend are allowable. Accordingly, Applicants request that the instant §103(a) rejections of the claims

CONCLUSION

In view of the foregoing amendments and remarks, it is believed that the applicable rejections have been overcome and all claims remaining in the application are

presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.

CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: 2/12/08

Mark R. Hennings
Reg. No. 48,982

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
Phone (206) 292-8600

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being transmitted electronically via EFS-Web to the United States Patent and Trademark Office on the date shown below.

Elizabeth J. Martinez 2-12-08
Date